REMARKS

Reconsideration and allowance in view of the foregoing amendments and the following remarks are respectfully requested.

New claims 9-16 have been added. Claims 3-4 and 7-8 have been amended. Claims 3-4 and 7-16 are pending in this application.

Drawings

The drawings stand objected to under 37 CFR1.83(a) because they fail to show the steps of removing the conductive material at a removal region and burying an interlayer dielectric film between the pattern at the removal region as described in the specification. Applicant herewith submits a replacement drawing for Figures 6A-6C. The amendments to the drawings have been made to make the drawings to be correspondent with the description in the specification. It is submitted that no new matter has been added in the replacement drawings. Withdrawal of the objection is respectfully requested.

Specification

In view of the Examiner's rejections to the specification, Applicant has amended the specification. Applicant submits that the specification is now in full compliance with 35 U.S.C. §112, first paragraph.

Claim Rejections – 35 U.S.C. §102

A. Claims 7 and 8 stand rejected under 35 U.S.C. §102(b) as being anticipated by Grewal et al. Applicant traverses the rejection for the following reasons.

Grewal et al. at least fails to disclose or suggest the step of removing a conductive material and insulating film spacers at a removal region such that the conductive material remains on a first contact plug to form a second contact plug and the insulating films spacers

remain at both sides of the second contact plug, as recited in claim 7, as amended. Grewal et al. shows no teaching regarding the second contact plug and the feature of removing the conductive material and the insulating film spacers at a removal region. As shown in Fig. 1I of Grewal et al., spacers remain at the sides of the gate structure. In addition, Grewal et al. simply fails to disclose the step of burying an interlayer dielectric film between the conductive layer patterns at the removal region.

Therefore, Applicant respectfully submits that claim 7 and its dependent claim 8 are not anticipated by Grewal et al. under 35 U.S.C. §102(b).

B. Claims 7 and 8 stand rejected under 35 U.S.C. §102(e) as being anticipated by Park et al. (US 6,753,252). Applicant traverses the rejection for the following reasons.

Park et al. also fails to disclose or suggest the step of removing the conductive material and the insulating film spacers at the removal region. As shown in the drawings and the specification, Park et al. shows spacers 26 formed on sidewalls of all gate structures 12 that include a region in which the contact plug 50 is not formed. Park et al. further fails to disclose or suggest the step of burying the interlayer dielectric film between the conductive layer patterns at the removal region.

Therefore, Applicant submits that claim 7 and its dependent claim 8 are not anticipated by Park et al. under 35 U.S.C. 102(e).

C. Claims 3-4 and 7-89 stand rejected under 35 U.S.C. §102(e) as being anticipated by Park et al. (US 6,387,759). Applicant traverses the rejection for the following reasons.

With regard to claim 7, Park et al. also fails to disclose or suggest at least the step of removing the conductive material and the insulating film spacers at the removal region. Like other references, Park et al. also shows spacers 212 formed on sidewalls of the gate 220 that includes a region in which contact plugs 216, 218 are not formed. Accordingly, Applicant submits that claim 7 and it's dependent claim 8 are not anticipated by Park et al. under 35 U.S.C. §102(e).

Claim 3 also recites a step of removing the conductive material and the insulating film spacers in the isolation region. It is submitted that Park et al. fails to disclose or suggest this limitation. It is also submitted that Park et al. fails to disclose or suggest the step of forming an interlayer dielectric film on an entire surface of the semiconductor device so that the interlayer dielectric film is buried between the conductive layer pattern in the isolation region.

Therefore, Applicant submits that claim 3 and its dependent claim 4 are not anticipated by Park et al. under 35 U.S.C. §102(e).

D. Claim 3 stands rejected under 35 U.S.C. §102(e) as being anticipated by Lee. Applicant traverses the rejection for the following reasons.

Lee not only fails to disclose or suggest the step of removing the conductive material and the insulating film spacers in the isolation region, but also fails to disclose or suggest the semiconductor substrate including a junction region and an isolation region. According to Lee, spacers 104, 106, 108 are not removed to expose the junction region and they remain in a region in which contact plug is not formed. In addition, the step of forming the interlayer dielectric film is not disclosed in Lee.

Therefore, claim 3 is not anticipated by Lee et al. under 35 U.S.C. §102(e).

E. Claim 3 stand rejected under 35 U.S.C. §102(e) as being anticipated by Jin et al. Applicant traverses the rejection for the following reasons.

Jin et al. also has similar deficiencies as other references cited by the Examiner. According to the Jin et al., spacers 208/210 remain in a region in which contact plug is not formed. Further, Jin et al. fails to disclose or suggest the semiconductor substrate including a junction region and an isolation region. Jin et al. is also moot in describing the step of forming the interlayer dielectric film. Therefore, Applicant respectfully submits that claim 3 is not anticipated by Jin et al. under 35 U.S.C. §102(e).

New Claims

Applicant submits that new claims 9-16 are also allowable over the references cited by the Examiner. In particular, none of the references discloses the step of removing the second conductive material and the second spacers on the first interlayer dielectric film and the step of forming a second interlayer dielectric film on the entire surface.

Conclusion

The prior art made of record and not relied upon is noted.

All objections and rejections having been addressed, it is respectfully submitted that claims 3-4 and 7-16 are now in condition for allowance and a notice to that effect is earnestly solicited. If any issues remain to be resolved, the Examiner is cordially invited to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

MAYER BROWN ROWE & MAW LLP

By: _____

Yoon S. Ham
Registration No. 45,307
Direct No. (202) 263-3280

YSH/jr
Intellectual Property Group
1909 K Street, N.W.
Washington, D.C. 20006-1101
(202) 263-3000 Telephone
(202) 263-3300 Facsimile
Date: May 15, 2006

FIG. 6A

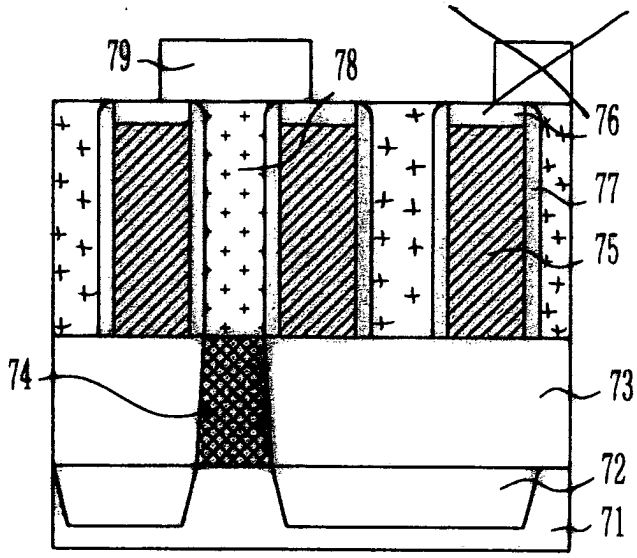


FIG. 6B

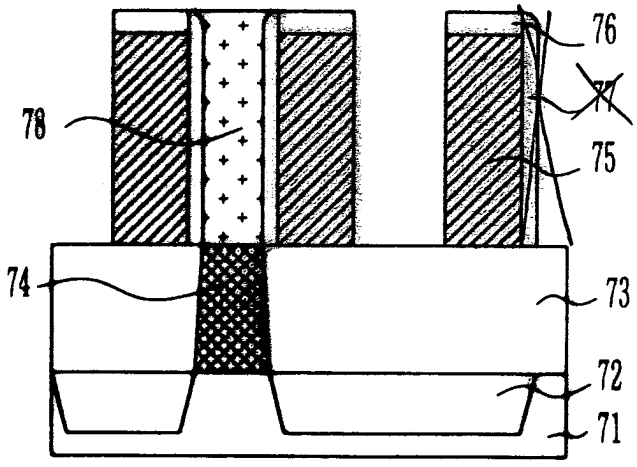
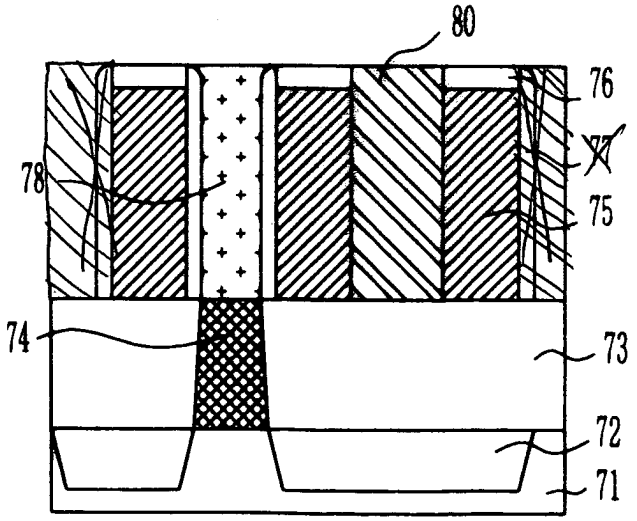


FIG. 6C



IN THE DRAWINGS

Please amend Fig. 6A-6C as attached replacement sheet.